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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/313,424	05/17/99	HUTTNER	GR-98-P-8041

EXAMINER	
KEDEBE, D	
ART UNIT	**PAPER NUMBER**
2823	

MNC2/0323

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DATE MAILED: 03/23/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

1- File Copy

Office Action Summary	Application No.	Applicant(s)	
	09/313,424	HUTTNER ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. This application contains claims 1-6 drawn to an invention nonelected without traverse in Paper No. 11. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Information Disclosure Statement

2. The information disclosure statement filed on September 7, 2000 of Paper No.7 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered. For the document No. 197 49 345 A1 of IDS Paper No. 7, which was not considered in Paper No. 12, there is no English abstract or English equivalence can be found in the application. Applicants are requested to resubmit the IDS with English abstract or English equivalence so that the Examiner can consider the citation.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the

passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer " as recited in claim 10 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7-9 and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu (US/5,468,657).

Re claim 7, Hsu teaches a method of fabricating a semiconductor configuration comprising: providing a semiconductor structure (see Fig. 4) having a base layer (44), an insulation layer (59), and a monocrystalline silicon layer (3); introducing a passivating substance X (not labeled) between the insulation layer (59) and the monocrystalline silicon layer (3); and heat-treating the semiconductor structure with the passivating substance X, thereby, causing the passivating substrate diffuse into an interface between the insulation layer (59) and the monocrystalline silicon layer (3) (see Fig. 4 and Col. 7, lines 24-45).

Re claim 8, as applied to claim 7 above, Hsu teaches all the claimed limitations including the limitation of ion-implanting the passivating substance X (see Fig. 4).

Re claim 9, as applied to claim 8 above, Hsu teaches all the claimed limitations including the limitation of defining an implantation maximum for the passivating substance X in vicinity of an interface between the insulation layer and the monocrystalline silicon layer (see Fig. 4).

Re claim 11, as applied to claim 7 above, Hsu teaches all the claimed limitations including the limitation of forming a covering oxide layer (68) on the monocrystalline silicon layer (see Fig. 5).

Re claim 12, as applied to claim 7 above, Hsu teaches all the claimed limitations including the limitation of patterning the monocrystalline silicon layer by etching away regions thereof down to the underlying insulation layer (see Fig. 5).

Re claim 13, as applied to claim 12 above, Hsu teaches all the claimed limitations including the limitation of patterning step is performed before the step of introducing the passivating substance X into one of the insulation layer and the monocrystalline silicon layer (see Fig. 5).

Re claim 14, as applied to claim 12 above, Hsu teaches all the claimed limitations including the limitation of patterning step is performed after the step of introducing the passivating substance X into one of the insulation layer and the monocrystalline silicon layer (see Fig. 5).

Re claim 15, as applied to claim 7 above, Hsu teaches all the claimed limitations including the limitation of doping the monocrystalline silicon layer differently region by region by means of ion implantation; and performing the doping step after the step of introducing the passivating substance X and the heat-treating step (see Col. 8, lines 17-67).

6. Claim10 is rejected under 35 U.S.C. 103(a) as being unpatentable Hsu (US/5,468,657).

as applied to claim 7 above, in view of Sato et al. (USPAT/5,854).

Re claim 10, as applied to claim 7 above, Hsu teaches all the claimed limitations including the limitation. Although the limitations of providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer is well-known in the art, Hsu does not disclose the claimed limitations. Sato et al. disclose providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer in order to form SOI (see Figs. 2A-2D). Sato et al. suggest that "formation of mono-crystalline Si semiconductor layer on an insulator is well known as silicon-on-insulator (SOI) technique. Many investigations have been made thereon since the devices made by the SOI technique have many advantages which are not

achievable with a bulk Si substrate for usual Si integrated circuits. The advantages brought about by the SOI technique are as below: 1. Ease of dielectric separation, and practicability of high integration, 2. High resistance against radioactive rays, 3. Low floating capacity, and practicability of high speed operation, 4. Practicability of omission of a welling step, 5. Practicability of prevention of latching-up, 6. Practicability of thin film formation for complete depletion type field effect transistor, and so forth." (see Sato et al. Col. 3, lines 42-59) One of ordinary skill in the art would have motivated to use SOI technique as Sato et al. disclosed in order to improve the overall device performance and applicability of the device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided , Kadosh et al. reference with SOI technique as taught by Sato et al. because the device performance would have been improved.

Response to Arguments

7. Applicants' arguments filed on February 1, 2001 in Paper No. 13 have been fully considered but they are not persuasive.

Regarding applicability of the *Sato et al.* as prior art, applicants argue that "Since the effective filing date of the instant application predates the application filling date of *Sato et al., Sato et al.* will not be available to be cited as prior art against the instant application." In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate because Sato et al. has well established U.S. priority dated back January 29, 1993. If the application is a continuation or divisional of one or more earlier U.S. applications and if the requirements of 35 U.S.C. 120 have been satisfied, the effective filing date is the same

as the earliest filing date in the line of continuation or divisional applications. See generaly MPEP § 706.

8. Applicants' arguments with respect to claims 7-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
March 21, 2001

Trung Dang
Primary Examiner